#8/Response 7-23-02

ASMEX.P[illegible]DV1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Raaijmakers et al.	Group Art Unit 2812
Appl. No.	:	09/764711	
Filed	:	January 18, 2001	
For	:	METHOD OF DEPOSITING SILICON WITH HIGH STEP COVERAGE	
Examiner	:	Angel Roman	

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: United States Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202, on

July 8, 2002
(Date)

Adeel S. Akhtar, Reg. No. 41,394

RESPONSE TO FINAL OFFICE ACTION

United States Patent and Trademark Office
P.O. Box 2327
Arlington, VA 22202

Dear Sir:

In response to the Final Office Action mailed on May 9, 2002, Applicants respectfully request reconsideration in view of the amendments and remarks below.

REMARKS

In the Final Office Action mailed on May 9, 2002, the Examiner rejected all pending claims. Applicants respectfully request reconsideration of the rejections in view of the remarks contained herein.

Anticipation Rejections

The Examiner has rejected Claims 33 and 35-37 as being anticipated by Vo (U.S. Patent No. 5,097,381A).

Regarding Vo, the Examiner stated that "Vo discloses an integrated capacitor formed in a trench having a width no more than about 0.25 micrometers … and an aspect ratio greater than about 20:1 (see column 5, lines 35-45), comprising; a dielectric layer 54 lining the trench; and a conductively doped polysilicon layer 52 (see column 5, lines 20-30) filling the trench."